

Abstract

A state control circuit (107) gives an inactive state control signal (S2) to a CPU (105) and an active state control signal (S3) to a data transmission circuit (102). In 5 response to this, the CPU (105) goes into the halt state and the data transmission circuit (102) goes into the receive state. When receive processing is completed, the state control circuit (107) gives an active state control signal (S2) to the CPU (105). In response to this, the CPU (105) 10 restores from the halt state to the operative state. The CPU (105) gives an instruction signal (CMD2) to the state control circuit (107). The state control circuit (107) gives an inactive state control signal (S3) to the data transmission circuit (102). In response to this, the data transmission 15 circuit (102) goes into the halt state.